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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOMMY HSIAO,
MARK T. RAMSBEY and YU SUN

Appeal 2008-0538
Application 10/689,298[1]
Technology Center 2800

Decided: December 16, 2008

Before ROBERT E. NAPPI, MARC S. HOFF, and KEVIN F. TURNER, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1, 3-9, and 17-26. We have jurisdiction under 35 U.S.C. § 6(b).

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[1] Application filed October 20, 2003. The real party in interest is Advanced Micro Devices, Inc.

We affirm, and enter a new ground of rejection.

Appellants' invention relates to a method and system for reducing short channel effects in a memory device, allowing for reduced gate lengths (Spec. 1). The invention provides for a drain implant after a source implant is driven under the first edge of each of a plurality of gate stacks (Spec. 6). The drain implant is subjected to less thermal cycling but still allows the source implant to be driven under the gate stack. The length of gates can be reduced, allowing for more memory cells to be fit in a given area (Spec. 7).

Claim 1 is exemplary:

1. A method for providing a semiconductor memory device including a substrate and at least one field isolation region, the method comprising the steps of:

(a) providing a plurality of gate stacks above the substrate, each of the plurality of gate stacks including a first edge and a second edge, each of the plurality of gate stacks crossing the at least one field isolation region;

(b) providing a source implant adjacent to the first edge of each of the plurality of gate stacks;

(c) driving the source implant under the first edge of each of the plurality of gate stacks;

(d) providing a drain implant after step (c), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Shah	US 5,065,208	Nov. 12, 1991
Miyata	US 5,183,773	Feb. 2, 1993
Chen	US 5,482,881	Jan. 9, 1996
Gardner	US 5,953,613	Sep. 14, 1999
Sun	US 6,235,584 B1	May 22, 2001

Claims 1, 3-5, 7, 8, 17, and 19-21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chen.

Claims 9, 24, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Gardner.

Claims 6 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Miyata.

Claims 22 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Shah.

Claims 1, 3, 4, 6-9, 17-19, and 24-26 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of Sun.

Claims 5, 20, and 21 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of Sun in view of Chen.

Claims 22 and 23 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of Sun in view of Shah.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Appeal Brief (filed October 17, 2005), the Reply Brief (filed March 15, 2006), and the Examiner's Answer (mailed January 11, 2006) for their respective details.

ISSUES

There are four principal issues in the appeal before us.

The first issue is whether Chen teaches providing a drain implant after driving a source implant under the first edge of each of the plurality of gate stacks (i.e., step (c) of claim 1), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks, as claim 1 requires.

The second issue is whether the skilled artisan would have been motivated to combine Chen and Gardner to arrive at the invention recited in claim 9.

The third issue is whether the skilled artisan would have been motivated to combine Chen and Miyata to arrive at the invention recited in claim 6.

The fourth issue is whether the skilled artisan would have been motivated to combine Chen and Shah to arrive at the invention recited in claim 22.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellants, the invention concerns a method and system for reducing short channel effects in a memory device, allowing for reduced gate lengths (Spec. 1). The invention provides for a drain implant after a source implant is driven under the first edge of each of a plurality of gate stacks (Spec. 6). The drain implant is subjected to less thermal cycling but still allows the source implant to be driven under the gate stack. The length of gates can be reduced, allowing for more memory cells to be fit in a given area (Spec. 7).

2. Appellants' Figure 1A, labeled 'Prior Art,' illustrates the provision of a first and second spacer (26, 28) along first and second edges of a plurality of gate stacks, respectively.

Chen

3. Chen teaches establishing a higher doping concentration in the tunneling regions of memory cells within an array by implanting an n+ dopant in the source region in two separate and distinct steps (col. 3, ll. 62-66).

4. Chen teaches an implant ("MDD2") in a drain region, adjacent to the second edge of each of the plurality of gate stacks (Chen Fig. 6E and col. 8, l. 61 to col. 9, l. 12).

5. Chen teaches disposing an oxide layer over an entire array of gate stacks (Fig. 6E, 720; col. 9, ll. 7-8; col. 10, ll. 1-2).

6. Chen teaches a selective etch that removes a portion of the substrate (Fig. 6, step 454; col. 7, ll. 59-61).

Gardner

7. Gardner teaches modifying the process flow for forming a MOSFET on a substrate, by only implanting a drain region and not the source during a source drain implant, second by forming silicon nitride spacers on the sides of a gate electrode, and third by supplying an electron source in the form of a metal plug adjacent to the spacer on the side of the gate electrode and abutting the substrate (col. 2, ll. 22-29).

8. Gardner teaches annealing a wafer following a drain implant, which achieves the advantages of activating the drain dopants and removing crystalline damage (col. 7, ll. 49-52)

Miyata

9. Miyata teaches a method of manufacturing a semiconductor device having an input protection transistor which is not destroyed even when supplied with a surge voltage or an overshoot voltage (col. 5, ll. 52-56).

Shah

10. Shah teaches fabricating integrated bipolar and CMOS devices, such that the steps for forming MOS transistors are made compatible and integrated with those of bipolar transistors (col. 2, ll. 9-16).

11. Shah teaches that it is known in the field of semiconductor device manufacturing to anneal a semiconductor wafer in order to drive an N type impurity of a source region under gate oxide (col. 10, ll. 33-37).

Sun

12. Sun teaches a method and system for providing a semiconductor memory device, including providing a drain implant after first source implant is driven under the first edge and after first and second spacers are provided (col. 3, ll. 52-56).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

In an appeal from a rejection for anticipation, the Appellants must explain which limitations are not found in the reference. *See Gechter v. Davidson*, 116 F.3d 1454, 1460 (Fed. Cir. 1997) ("[W]e expect that the Board's anticipation analysis be conducted on a limitation by limitation basis, with specific fact findings for each *contested* limitation and satisfactory explanations for such findings.")(emphasis added). *See also In*

re Kahn, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious. In particular, the Supreme Court emphasized that "the principles laid down in *Graham* reaffirmed the 'functional approach' of *Hotchkiss*, 11 How. 248." *KSR,* 127 S. Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966) (emphasis added)), and reaffirmed principles based on its precedent that "[t]he combination of familiar

elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The Court explained:

> When a work is available in one form of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 1740. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

"Under the correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the patent [or application at issue] can provide a reason for combining the elements in the manner claimed. " *KSR*, 127 S. Ct. at 1742.

The determination of obviousness must consider, *inter alia*, whether a person of ordinary skill in the art would have been motivated to combine the prior art to achieve the claimed invention and whether there would have been a reasonable expectation of success in doing so. *Brown & Williamson Tobacco Corp. v. Philip Morris, Inc.*, 229 F.3d 1120, 1124 (Fed. Cir. 2000). *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1164 (Fed. Cir. 2006). Where the teachings of two or more prior art references conflict, the Examiner must weigh the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588,

591 (Fed. Cir. 1991). If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984). Further, our reviewing court has held that "[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994); *Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc.,* 73 F.3d 1085, 1090 (Fed. Cir. 1995).

ANALYSIS

Claims 1, 3, 7, 8, and 17

We select claim 1 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellants argue that Chen does not meet the limitation of "providing a drain implant after step (c), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks," recited in claim 1, because the MDD2 implant taught by Chen is "clearly performed simultaneously on the source and the drain" (Br. 5). Because each mention of "'source implant'" and "'drain implant'" in the Specification is mutually exclusive (Br. 5), and there is no mention of the drain implant being performed on both the source and the drain (Br. 6), Appellants argue, Chen cannot anticipate the claim.

Appellants' arguments are not persuasive of error by the Examiner. Because Appellants' Specification contains no special definition of the

phrase "drain implant," we must accord the phrase a meaning consistent with its usage in the pertinent art, as an implant of ions in the drain region of a transistor formed on a semiconductor substrate.

The Examiner found, and Appellants do not contest, that Chen teaches such an implant ("MDD2") in such a drain region, adjacent to the second edge of each of the plurality of gate stacks (Ans. 4; FF 4). It is immaterial that Chen's MDD2 implant also impacts a source region, because the plain language of claim 1 does not exclude the possibility of such an impact. We therefore find that Chen teaches providing a drain implant in the substrate adjacent to the second edge of each of the plurality of gate stacks, as called for in claim 1.

Because Appellants have not persuaded us that the Examiner has erred in finding that Chen teaches all of the elements of the invention recited in claim 1, we sustain the Examiner's rejection of claim 1, as well that of claims 3, 7, 8, and 17 not separately argued, under 35 U.S.C. § 102.

Claims 19-21

We select claim 19 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellants' arguments for the patentability of claim 19 are the same arguments made for the patentability of claim 1. Because we find *supra* that Chen teaches all the limitations of claim 1, then, we also find that Chen teaches all the limitations of claim 19, for the same reasons.

We therefore sustain the Examiner's rejection of claim 19, and of claims 20 and 21 not separately argued, under 35 U.S.C. § 102.

Claim 4

Appellants argue that Chen does not anticipate claim 4, dependent from claim 1, for the further reason that Chen does not teach providing a first spacer and a second spacer, each disposed along a respective edge of the plurality of gate stacks. Appellants argue that because Chen's insulating layer (720) is "an oxidation sealing layer that is grown over the entire array of gate stacks" (Ans. 13), Chen cannot meet the limitations of claim 4.

Appellants' arguments are persuasive of Examiner error. The Examiner asserts that claim 4 "does not require the spacer or the layer the spacer is formed from to not extend over the gate stacks" (Ans. 14). Though the Examiner is literally correct, we are not persuaded by the Examiner's position that disposing an oxide layer over the entire array of gate stacks (FF 5), without the teaching of any etching to form "spacers" as the term is understood in the art, would meet the claim. A "spacer" would necessarily function to separate, or provide space between, two elements; an undifferentiated oxide layer over the entire array does not function in such a manner.

We therefore find that Chen does not teach all the limitations of claim 4. Accordingly, we will not sustain the Examiner's rejection of claim 4 under 35 U.S.C. § 102.

Claim 5

Appellants argue that Chen does not teach the claimed "'self-aligned source etch'" because the etch cited by the Examiner is "a selective etch performed after masking the drain regions, but before any implant steps have been performed" (Br. 7).

Appellants' argument is not persuasive of Examiner error. Chen teaches a selective etch that corresponds to the claimed source etch (FF 6). We agree with the Examiner that claim 5 does not require that the self-aligned source etch be performed at any particular point during the fabrication sequence (Ans. 14). Therefore, Appellants' arguments have not persuaded us that the Examiner erred in finding that Chen teaches all the limitations of claim 5, and sustain the Examiner's rejection of claim 5 as being unpatentable under 35 U.S.C. § 102.

Claims 9, 24, and 25

We select claim 9 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellants argue that the Examiner has not supplied proper motivation to combine Chen with Gardner, because "*Gardner* teaches away from implanting the source region of the substrate, whereby [sic] the present invention teaches providing a drain implant after driving the source implant" (Br. 11). Appellants further argue that the Examiner's rejection is based upon impermissible hindsight, because Chen does not teach the drain implant claimed in Appellants' invention (Br. 12).

Appellants' argument is not persuasive of error by the Examiner. Gardner is not relied upon to teach implanting a source region, but merely to teach annealing a wafer following a drain implant, which achieves the advantages of activating the drain dopants and removing crystalline damage (FF 8). Whether Gardner teaches away from implanting the source region of a substrate is therefore not relevant to patentability.

We find that Gardner teaches the annealing step conceded to be missing from Chen, and that Gardner supplies motivation to modify Chen in

the manner suggested by the Examiner. Because we find *supra* that Chen teaches the drain implant claimed by Appellants, we find that the Examiner did not engage in impermissible hindsight reconstruction, because Gardner supplies reasons to anneal a semiconductor wafer following a drain implant.

We therefore sustain the rejection of claim 9, as well as claims 24 and 25 not separately argued, under 35 U.S.C. § 103.

Claims 6 and 26

We select claim 6 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellants argue that the Examiner lacks motivation to make the asserted combination of Chen and Miyata, because Miyata does not teach providing a drain implant after a source implant has been driven (Br. 13). Appellants further argue that Miyata does not disclose a memory device that suffers from short channel effects, nor teach driving a drain or source implant under the edge of a gate stack (Br. 13-14).

Appellants' arguments are not persuasive of error by the Examiner. Because we find *supra* that Chen teaches providing a drain implant after a source implant has been driven (see the discussion of claim 1), the lack of teaching of such an implant does not render the rejection of claim 6 erroneous. Appellants do not contest that Chen teaches driving a source implant under the first edge of each of the plurality of gate stacks (Ans. 4). Finally, Appellants' discussion of short channel effects is not germane to the claimed invention, because claim 6 makes no mention of short channel effects.

We therefore sustain the Examiner's rejection of claim 6, as well as that of claim 26 not separately argued, as being unpatentable under 35 U.S.C. § 103.

Claims 22 and 23

We select claim 22 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellants argue that the Examiner's stated motivation to combine Chen and Shah fails because Shah is not directed to semiconductor memory, Shah does not mention providing a drain implant after a source implant has been driven, Shah cannot be considered analogous art with the present invention (Br. 16). Appellants further argue that the Examiner is engaging in impermissible hindsight reconstruction because Shah teaches annealing the source and drain of a logic transistor, rather than "a semiconductor memory source implant" (Br. 17).

Appellants' arguments fail to establish that the rejection is in error. Because we find *supra* that Chen teaches providing a drain implant after a source implant has been driven (see the discussion of claim 1), the lack of teaching of such an implant does not render the rejection of claim 22 erroneous. Because Shah teaches that it is known in the field of semiconductor device manufacturing to anneal a semiconductor wafer in order to drive an N type impurity of a source region under gate oxide (FF 11), we conclude that Shah does constitute analogous art and can provide a reason to modify Chen to achieve the claimed invention. *See KSR*, 127 S. Ct. at 1742. Similarly, because we conclude that Shah constitutes analogous art, we do not consider the Examiner to be reliant upon hindsight in combining Chen and Shah in the manner proposed.

We therefore sustain the rejection of claim 22, as well as that of claim 23 not separately argued, under 35 U.S.C. § 103.

Double Patenting Rejection of claims 1, 3-9, and 17-26

Appellants do not contest the Examiner's double patenting rejections, stating their intention to file a Terminal Disclaimer upon the allowance of claims 1, 3-9, and 17-26 (Br. 17). We therefore sustain pro forma the Examiner's double patenting rejections of claims 1, 3-9, and 17-26.

Rejection of claim 4 under 37 C.F.R. § 41.50(b)

We make the following new grounds of rejection using our authority under 37 C.F.R. § 41.50(b).

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Appellants' Admitted Prior Art (APA).

As noted *supra*, we find that Chen teaches each of the limitations of parent claim 1, and that Chen does not teach providing first and second spacers along respective edges of gate stacks, as claim 4 requires. Appellants' Figure 1A is admitted to be Prior Art and illustrates the provision of a first and second spacer (26, 28) along first and second edges of a plurality of gate stacks, respectively (FF 2). It would have been obvious to the skilled artisan to modify Chen, e.g., by etching, to form the spacers taught by APA, for the benefit of providing insulation between adjacent gate stacks and because Appellants' Figure 1A illustrates that such spacers are generally known and are typically used in memory devices such as are taught by Chen.

CONCLUSIONS OF LAW

Chen teaches providing a drain implant after driving a source implant under the first edge of each of the plurality of gate stacks (i.e., step (c) of claim 1), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks, as claim 1 requires.

The skilled artisan would have been motivated to combine Chen and Gardner to arrive at the invention recited in claim 9.

The skilled artisan would have been motivated to combine Chen and Miyata to arrive at the invention recited in claim 6.

The skilled artisan would have been motivated to combine Chen and Shah to arrive at the invention recited in claim 22.

ORDER

The Examiner's rejection of claims 1, 3-9, and 17-26 is affirmed. The Examiner's rejection of claim 4 under 35 U.S.C. § 103 is reversed.

We have also entered a new ground of rejection against claim 4 under 37 C.F.R. § 41.50(b).

37 C.F.R. § 41.50(b) provides that, "[a] new grounds of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, *WITHIN TWO MONTHS FROM THE DATE OF THE DECISION*, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter

reconsidered by the examiner, in which event the proceeding will be remanded to the examiner …

(2) Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record …

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

37 C.F.R. § 41.50(b)

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